AD9625 Evaluation Board Quick Start Guide

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Quick Start Guide for testing the AD9625 ADC Evaluation Board using the FPGA based Capture Board (HSC-ADC-EVALEZ)

TYPICAL SETUP

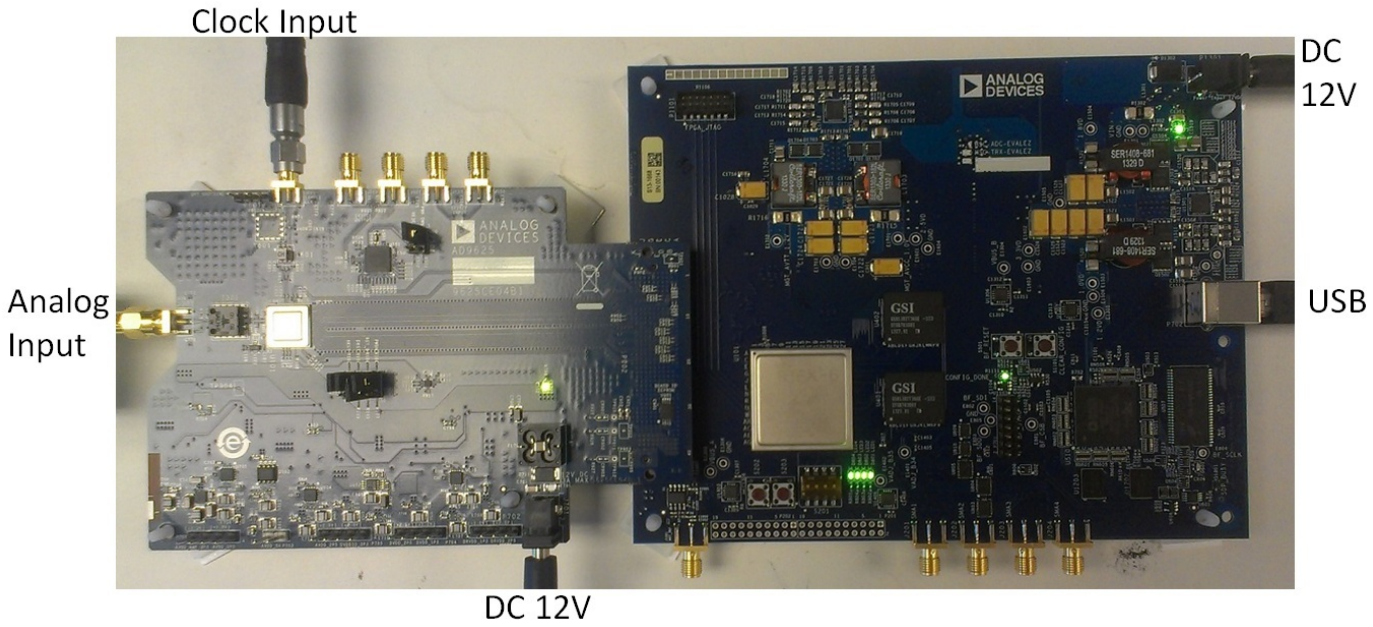

Figure 1. AD9625 Evaluation Board (Left) and HSC-ADC-EVALEZ Data Capture Board (Right)

EQUIPMENT NEEDED

- AC to 12V DC power supplies (2)
- Analog signal source, anti-aliasing filter and SMA cable.
- Clock source and SMA cable.
- PC running Windows
- USB 2.0 cable
- AD9625 Evaluation Board
- HSC-ADC-EVALEZ FPGA Based Data Capture Board

HELPFUL DOCUMENTS

- AD9625 Datasheet
- VisualAnalog Converter Evaluation Tool User Manual, AN-905
- High Speed ADC SPIController Software User Manual, AN-878
- Interfacing to High Speed ADCs via SPI, AN-877

SOFTWARE NEEDED

- VisualAnalog
- SPIController

ANALOG OPTION

- Single-Ended to Differential Balun input to AD9625

All documents and software are available at http://www.analog.com/fifo.
For any questions please send an email to highspeed.converters@analog.com.

TESTING

1. Connect the AD9625 evaluation board and the HSC-ADC-EVALEZ board together with the FMC connector as shown in Figure 1. Do not change any jumper settings on the evaluation board.

3. Connect one12V AC/DC power supply to HSC-ADC-EVALEZ.

4. Connect one12V AC/DC power supply to the AD9625 evaluation board.

5. Connect the HSC-ADC-EVALEZ board to the PC with a USB cable.

6. Provide a clean, low-jitter source to the clock input. The input clock level at the connector should be between 500 and 2000mVpp.

7. Open the VisualAnalog software tool on the PC.

8. Select AD9625 and the template that corresponds to the type of testing that needs to be performed.

9. Select the ADC Data Capture Settings window and click on the 'Capture Board' tab. In the FPGA box select program to configure the FPGA.

10. On the ADC evaluation board, use a clean signal generator with low phase noise to provide an analog input signal.

11. Open the SPIController software tool on the PC. Click 'ignore' if you see the "CONFIGURATION FILE ERROR". Check the title bar of the window to see which configuration is loaded. If necessary, choose "Cfg Open" from the "File" menu and select the AD9625 configuration file.

12. Click the New DUT button () in SPI Controller.

13. Ensure that there is no analog input signal.

14. Ensure that the encode clock is running. Based on the desired sample clock rate, select the appropriate Quick Configuration Value from the table below. The default case is 'Generic 8 lane'. The Quick Configuration Value is set in register 0x5E at the top of the ADCBase1 tab in the SPIController tool.

Quick Configuration Value	Sample Clock	
	(Min MSPS)	(Max MSPS)
Generic: 2 lanes	330	650
Generic: 4 lanes	650	1300
Generic: 8 lanes	1300	2000

15. Click the Run button  or Continuous Run button  in VisualAnalog.

16. Adjust the amplitude of the input signal so that the fundamental is at the desired level. (Examine the "Fund Power" reading in the left panel of the VisualAnalog FFT window.)

17. If desired, click on File>Save Form as in the FFT window to save the FFT plot.